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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,250	04/08/2004	Gary D. Sasser	15436.253.82.1	7500

22913 7590 01/08/2007

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EXAMINER	
LEUNG, CHRISTINA Y	
ART UNIT	**PAPER NUMBER**
2613	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/820,250	SASSER ET AL.	
	Examiner	Art Unit	
	Christina Y. Leung	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :11-23-04; 1-31-05; 9-20-05; 10-05-05; 10-24-05; 2-03-06.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 4-6, 8-17, 19-21, 23-29, 31-39, 41, 42, and 44-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aronson et al. (US 2002/0149821 A1) in view of Gilliland et al. (US 2002/0181894 A1).

Regarding claim 1, Aronson et al. disclose an optoelectronic module 100 (Figure 2), comprising:

an optoelectronic component (including receiver 102 and transmitter 103);

a controller IC (shown in Figure 2 as another element "102," but shown in Figure 3 and referred to in the text as element 110) including a serial digital interface (element 121 in Figure 3) configured to facilitate communication, between the optoelectronic module and a host, of diagnostic parameter information concerning the optoelectronic component (paragraphs [0027], [0028], and [0035]); and

a pinout arrangement comprising:

a pin array having a plurality of pins, at least some of which are in communication with the controller IC (Figure 2 shows pins 12-19, for example; paragraphs [0013]-[0014]); and

a pair of pins in communication with the serial digital interface (pins 15 and 16 shown in Figures 2 and 3), each of the pair of pins also being configured and arranged for communication with the host by way of a corresponding interface line (paragraph [0028]).

Aronson et al. do not specifically disclose that the module includes a housing or that the optoelectronic component and controller IC are disposed within the housing. However, Gilliland et al. teach an optoelectronic module (Figure 3) related to the one disclosed by Aronson et al. including an optoelectronic component (receiver 31 and laser 32) and a controller IC (such as power control element 48). They further teach disposing these module elements within a housing (Figures 1a-e; paragraphs [0034]-[0035].

It would have been obvious to a person of ordinary skill in the art to place the elements disclosed by Aronson et al. in a housing as taught by Gilliland et al. in the module in order to protect the components from the external environment.

Regarding claim 17, Aronson et al. disclose an optical transceiver module (Figure 2), comprising:

a transmit optical subassembly 103;

a receive optical subassembly 102;

a controller IC (shown in Figure 2 as another element "102," but shown in Figure 3 and referred to in the text as element 110) including:

a serial digital interface 121 configured and arranged to facilitate communication, between the optical transceiver module and a host, of diagnostic parameter information relating to at least one of: the transmit optical subassembly; and, the receive optical subassembly (paragraphs [0027], [0028], and [0035]); and

a plurality of memory mapped locations, at least one of which is configured to store diagnostic parameter information and is accessible by way of the serial digital interface (paragraphs [0035]-[0036]); and

a pinout arrangement comprising:

a pin array having a plurality of pins, at least some of which are in communication with the controller IC (Figure 2 shows pins 12-19, for example; paragraphs [0013]-[0014]); and

a pair of pins in communication with the serial digital interface (pins 15 and 16 shown in Figures 2 and 3), each of the pair of pins also being configured and arranged for communication with the host by way of a corresponding interface line (paragraph [0028]).

Again, Aronson et al. do not specifically disclose that the module includes a housing or that the transmit and receive subassemblies and controller IC are disposed within the housing. However, Gilliland et al. teach an optoelectronic module (Figure 3) related to the one disclosed by Aronson et al. including an optoelectronic component (receiver 31 and laser 32) and a controller IC (such as power control element 48). They further teach disposing these module elements within a housing (Figures 1a-e; paragraphs [0034]-[0035].

It would have been obvious to a person of ordinary skill in the art to place the elements disclosed by Aronson et al. in a housing as taught by Gilliland et al. in the module in order to protect the components from the external environment.

Regarding claim 38, Aronson et al. disclose an optoelectronic module (Figure 2), comprising:

an optoelectronic component (including receiver 102 and transmitter 103);

a controller IC disposed within the housing (shown in Figure 2 as another element "102," but shown in Figure 3 and referred to in the text as element 110) and including a serial digital interface 121 configured to facilitate communication, between the optoelectronic module and a host, of diagnostic parameter information concerning the optoelectronic component (paragraphs [0027], [0028], and [0035]); and

a pinout arrangement comprising:

a pin array ((Figure 2 shows pins 12-19, for example); and

a pair of pins in communication with the serial digital interface (pins 15 and 16 shown in Figures 2 and 3), each of the pair of pins also being configured and arranged for communication with the host by way of a corresponding interface line (paragraph [0028]).

Again, Aronson et al. do not specifically disclose that the module includes a housing or that the optoelectronic component and controller IC are disposed within the housing. However, Gilliland et al. teach an optoelectronic module (Figure 3) related to the one disclosed by Aronson et al. including an optoelectronic component (receiver 31 and laser 32) and a controller IC (such as power control element 48). They further teach disposing these module elements within a housing (Figures 1a-e; paragraphs [0034]-[0035].

It would have been obvious to a person of ordinary skill in the art to place the elements disclosed by Aronson et al. in a housing as taught by Gilliland et al. in the module in order to protect the components from the external environment.

Further regarding claim 38, Aronson et al. also do not specifically disclose that the pin array has pins configured and arranged for substantial conformity with the SFF configuration standard. However, it is well understood in the art that a physical arrangement of pins in a module may be designed to conform to an industry standard in order to ensure that the module is compatible with other devices (such as with the host device already by Aronson et al.). Gilliland et al. also specifically suggest that connectors in an optoelectronic module may conform to a SFF standard (paragraph [0002]).

It would have been obvious to a person of ordinary skill in the art to ensure that the pins in the module disclosed by Aronson et al. conform to a standard such as the SFF configuration standard as taught by Gilliland et al. in order to ensure that the module is compatible with other components in a larger system. One in the art would have been particularly motivated to ensure compatibility since Aronson et al. already discloses that the module communicates with at least a host device and must be connected somehow to other devices.

Regarding claims 6 and 21, Aronson et al. in view of Gilliland et al. describe systems as discussed above with regard to claims 1 and 17 above. As similarly discussed above with regard to claim 38, Aronson et al. do not specifically disclose that the pin array has pins configured and arranged for substantial conformity with the SFF configuration standard. However, it is well understood in the art that a physical arrangement of pins in a module may be designed to conform to an industry standard in order to ensure that the module is compatible with other devices (such as with the host device already by Aronson et al.). Gilliland et al. also specifically suggest that connectors in an optoelectronic module may conform to a SFF standard (paragraph [0002]).

Regarding claims 6 and 21, it would have been obvious to a person of ordinary skill in the art to ensure that the pins in the module described by Aronson et al. in view of Gilliland et al. conform to a standard such as the SFF configuration standard as taught by Gilliland et al. in order to ensure that the module is compatible with other components in a larger system. One in the art would have been particularly motivated to ensure compatibility since Aronson et al. already discloses that the module communicates with at least a host device and must be connected somehow to other devices.

Regarding claims 2 and 39, Aronson et al. discloses that the optoelectronic component comprises a transmit optical subassembly 103 and a receive optical subassembly 102.

Regarding claims 4, 19, and 41, Aronson et al. disclose that the controller IC is configured to receive from the host, by way of at least one of the pair of pins, at least one of the following: a command; data; and, diagnostic parameter information (paragraph [0028]).

Regarding claims 5, 20, and 42, Aronson et al. disclose that one of the pair of pins is configured to communicate with the host by way of an SDA interface line, and the other of the pair of pins is configured to communicate with the host by way of an SCL interface line (paragraph [0028]).

Regarding claims 8 and 23, Aronson et al. disclose that the diagnostic parameter information includes at least one of: warning information; alarm information; and, status information (paragraphs [0035], [0038], and [0039]).

Regarding claims 9, 24, and 45, Aronson et al. disclose that one of the pair of pins comprises a serial communication data pin, and the other of the pair of pins comprises a serial communication clock pin (paragraph [0028]).

Regarding claims 10 and 25, Aronson et al. in view of Gilliland et al. describe systems as discussed above with regard to claims 1 and 17. Aronson et al. disclose a pair of pins 15 and 16 for communicating with a host device by way of a corresponding interface, but they do not specifically disclose that the pair of pins is configured for repeated pluggability. However, Gilliland et al. also specifically further teach pins used to connect to a host device that are configured for repeated pluggability (paragraphs [0002] and [0046]).

Regarding claims 10 and 25, it would have been obvious to a person of ordinary skill in the art to configure the pins for pluggability as taught by Gilliland et al. in the systemd escribed by Aronson et al. in view of Gilliland et al. in order to ensure that the devices may easily connect and reconnect to various other components in the context of a larger system. One in the art would have been particularly motivated to ensure that the pins are pluggable as taught by Gilliland et al., since Gilliland et al. teach pluggable pins as part of a GBIC standard (Gilliland et al, paragraph [0002] and Aronson et al. also already disclose the serial digital interface corresponding to the pair of pins substantially conforms to a GBIC standard (Aronson et al., paragraph [0028])

Regarding claim 11, Aronson et al. disclose that the controller IC is configured to generate at least one of a temperature dependent output and a temperature independent output (paragraphs [0033] and [0034]). Although Aronson et al. specifically disclose both "temperature dependent" and "temperature independent" outputs using those terms, Examiner respectfully notes that any output of a controller IC would necessarily be "at least one of" a temperature dependent output and a temperature independent output, since they are mutually exclusive selections.

Regarding claim 12, Aronson et al. disclose that the controller IC further comprises an analog monitoring connection (paragraph [0035]).

Regarding claim 13, Aronson et al. disclose that the serial digital interface substantially conforms to a GBIC standard (paragraph [0028]).

Regarding claims 14 and 32, Aronson et al. disclose that the optoelectronic module is configured to receive a "rate select" signal from the host by way of one of the pins of the pinout arrangement (paragraph [0045]).

Regarding claim 33, Aronson et al. disclose that the "rate select" signal includes at least "high" and "low" values, each of which corresponds to a different data rate (paragraph [0045]).

Regarding claim 34, Aronson et al. disclose that the "rate select signal" is received from the host by way of one of the pair of pins (Aronson et al. discloses that the signal is received via the host interface, which comprises the pair of pins 15 and 16; paragraphs [0028] and [0045]).

Regarding claims 15 and 35, Aronson et al. disclose that the optoelectronic module is configured to transmit a "transmitter fault" signal to the host by way of one of the pins of the pinout arrangement (paragraph [0040]).

Regarding claim 36, Aronson et al. disclose that the "transmitter fault" signal is transmitted to the host by way of one of the pair of pins (Aronson et al. discloses that the signal is transmitted via the host interface, which comprises the pair of pins 15 and 16; paragraphs [0028] and [0040]).

Regarding claim 26, Aronson et al. disclose that at least one of the plurality of memory mapped locations is implemented as a register (paragraphs [0029] and [0030]).

Regarding claims 16, 27, and 46, Aronson et al. disclose a plurality of memory mapped locations, at least one of which is accessible by way of the serial digital interface and disclose that at least one of the plurality of memory mapped locations is configured to be read, and written to, by way of the serial digital interface. (paragraph [0028]). Further regarding claim 46 in particular, Aronson et al. also disclose that at least one of the plurality of memory mapped locations is accessible by way of the serial digital interface and which is configured to receive and store information concerning at least one diagnostic parameter (paragraph [0028]).

Regarding claim 28, Aronson et al. disclose that at least one of the memory mapped locations is configured to receive and store information concerning at least one of: a bias current associated with the transmit optical subassembly; optical transmit power associated with the transmit optical subassembly; and received signal power (paragraph [0036]).

Regarding claim 29, Aronson et al. disclose that the diagnostic parameter information stored in the at least one memory mapped location is in a digitized form (paragraph [0036]),

Regarding claim 31, Aronson et al. disclose that the module may include one or more of: a laser driver; a laser bias controller; a power controller; a pre-amplifier; a post-amplifier; a laser wavelength controller; a main controller; an electrothermal cooler; an analog-to-digital converter; a digital-to analog converter; and, an avalanche photodiode bias controller (Figure 2 shows a post amplifier and a laser driver, for example).

Regarding claim 37, Aronson et al. disclose that a memory map table associated with at least one of the plurality of memory map locations comprises information indicating at least one of: a storage location of a measured value of a diagnostic parameter; a storage location of a limit value for a diagnostic parameter; a storage location of a flag value for a diagnostic parameter;

and, a storage location of a configuration value for a diagnostic parameter (paragraphs [0027] and [0036]).

Regarding claim 44, Aronson et al. disclose that the diagnostic parameter information comprises at least one of: a bias current associated with the optoelectronic component; optical transmit power associated with the optoelectronic component; and received signal power associated with the optoelectronic component (paragraph [0036]).

3. Claims 3, 18, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aronson et al. in view of Gilliland et al. as applied to claims 1, 17, and 38 above, and further in view of Keevill et al. US 6,359,938 B1.

Regarding claims 3, 18, and 40, Aronson et al. in view of Gilliland et al. describe systems as discussed above with regard to claims 1, 17, and 38, including a serial digital interface. Aronson et al. do not specifically disclose I2C or MDIO serial communication.

However, various serial interface standards are well known in the communications art, and Aronson et al. already further disclose that the serial digital interface may be compatible with various types of serial interface standards (paragraph [0028]). Keevill et al. in particular teach a system that is related to the one described by Aronson et al. in view of Gilliland et al. including a communications device 146 that communicates with a host device via a serial interface 142 (Figure 12). Keevill et al. further teach that the serial interface is compatible with I2C serial communication (Figure 55; column 37, lines 1-8).

Regarding claims 3, 18, and 40, it would have been obvious to a person of ordinary skill in the art to use a I2C serial communication standard as taught by Keevill et al. in the system described by Aronson et al. in view of Gilliland et al. as an engineering design choice of a serial

communication standard in order to allow the system to properly communicate with a particular host device as already disclosed by Aronson et al. Again, Aronson et al. already disclose that the serial digital interface may be compatible with various serial interface standards (paragraph [0028]).

4. Claims 7, 22, 30, and 43 rejected under 35 U.S.C. 103(a) as being unpatentable over Aronson et al. in view of Gilliland et al. as applied to claims 1, 17, and 38 above, and further in view of Baltz et al. (US 6,469,906 B1).

Regarding claims 7, 22, 30, and 43, Aronson et al. in view of Gilliland et al. describe systems as discussed above with regard to claim 1, 17, and 38, including a pin array, and Gilliland et al. further suggest that connectors in an optoelectronic module may conform to a SFF standard (paragraph [0002]).

Regarding claims 7, 22, and 43 in particular, neither Aronson et al. nor Gilliland et al. specifically disclose or suggest that the pin array comprises one of: a 2x5 pin arrangement; and, a 2x10 pin arrangement.

Regarding claim 30 in particular, neither Aronson et al. nor Gilliland et al. specifically disclose or suggest that the pin array comprises two rows or six pins each. However, Aronson et al. already disclose that the pin array comprises pins, wherein each pin comprises one of the following: a serial communication data pin; a receiver ground pin; a receiver power pin; a signal detect pin; a receive data inverted pin; a receive data pin; a serial communication clock pin; a transmitter power pin; a transmitter ground pin; a transmitter disable pin; a transmit data pin; a transmit data inverted pin; an interrupt pin; and a loss of signal pin (Figure 2 shows the various types of pins in the pin array; see also paragraphs [0027]-[0028]). neither Aronson et al.

Further regarding claims 7, 22, 30, and 43, it is well understood in the art that a physical arrangement of pins in a module may be designed to conform to an industry standard such as already suggested by Gilliland et al. in order to ensure that the module is compatible with other devices (such as the host device already by Aronson et al.).

Baltz et al. further suggest an optical transceiver module, that is related to the ones disclosed and suggested by Aronson et al. and Gilliland et al., and that may conform to a SFF standard and have pin array comprising a 2x5 or a 2x6 pin arrangement (based on conforming to that standard; column 1, lines 52-65).

Regarding claims 7, 22, 30, and 43, it would have been obvious to a person of ordinary skill in the art to ensure that the pins in the module disclosed by Aronson et al. conform to a standard such as the SFF configuration standard as taught by Gilliland et al. and Baltz et al. (with a 2x5 or 2x6 pin array arrangement as taught by Baltz et al.) in order to ensure that the module is compatible with other components in a larger system.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christina Y. Leung whose telephone number is 571-272-3023. The examiner can normally be reached on Monday to Friday, 6:30 to 3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on 571-272-3022. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christina Leung
CHRISTINA LEUNG
PRIMARY EXAMINER